Plans for Si-Based SET Pump at NIST Gaithersburg

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`/home/neilz/experimental/THOUGHTS/SI_SET/4plans_5_01.tex`

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0.1 Motivation and Basic Idea

We would like to get a current standard which is both: i) based on 1 e, and ii) delivers much more than 1 pA.

Various groups are trying different approaches to this, including:

1. superconducting pump - NIST Boulder
2. smaller C in normal metal - NIST Boulder
3. SAW-SET
4. RF-SETT to count electrons

Another obvious approach is to parallelize a large number of pumps. This is made inconvenient or difficult by the charge offset problem, especially the time-dependent part. Recently, we have done measurements of NTT-made Si-SETT's, which apparently have no time-dependent drift (although they may have a static Q_0). This encourages us to attempt to make a SET pump in Si. Among the advantages are:

1. no charge offset drift - easier to use one
2. no charge offset drift - possible to parallelize

3. smaller C - higher temperature?

4. smaller C - faster?

Among the disadvantages are:

1. We have no experience in Si-based devices.

2. There may be more difficulty in getting uniformity in Si-based; this will be an important topic of research.

Based on a literature review I have made of the Si-SET field, I believe the following points are important:

ease of fabrication and uniformity A main driver for this field is room-temp operation; since this is not so crucial for us, we can accept larger size, which I hope will make fab easier, and allow better uniformity.

Q_0 our work with a **particular** Si-SET, that made by NTT, suggests that at least the inversion layer type of device is drift-free.

Q_0 in highly-doped wires, there is common speculation, and at least one report[1], that TLF's exist.

formation of TJ's – electrostatic The Korean group has demonstrated this[2][3]. However, they had fairly poor uniformity[3], and have only published one paper with work above 15 mK (at 4.2 K). More recently (early 2004), measurements here at NIST on the NTT devices have shown nice transistor action and good uniformity (capacitances within 15 %) using electrostatically-gates devices.

fabrication The U. Tokyo group has shown a really nice way to make **uniform**, narrow Si wires, with a double-TMAH-etch trick.

uniformity is a big issue

1. NTT is problematic - 1/10 yield earlier on PADOX devices, better recently.
2. U Tokyo – no way to know, but they've stopped publishing.
3. Korean group – electrostatic inversion – looks bad in *single* device.

0.2 Important Criteria for Devices

1. Low leakage - high resistance when MOSFET is off. We need about $10^{20}\Omega$, or greater (at low temperature, 4 K or less).

2. Small size - if we can get the wire width and the gate lengths and separations all less than or about 40 nm, that would be acceptable. If we could get them even smaller, to 20 - 30 nm, that would help more, but might not be worth the additional effort. This push is because, the smaller the sizes, the smaller the total capacitance, and thus the larger the maximum operation frequency, and the higher the maximum operation temperature.

3. Uniformity/homogeneity - we want the wire to be as regular and well-formed along its length as possible, and the devices to be as homogeneous as possible, so that the various gate capacitances are as uniform

as possible for multiple devices. 10% would be a good target for maximum non-uniformity.

4.

0.3 Experimental Plans

1. SETT: make an electrostatically-defined transistor.
2. SETT Q_0 drift: is there any?
3. SETT uniformity: how uniform can we make devices?
4. multiple dot: can we a multidot SETT?
5. multiple dot: can we make and operate a pump?
6. pump: operation? max freq? error rate? max temp?
7. pump uniformity: how similar can we make pulses for one pump?
8. pump uniformity: how similar can we make multiple pumps?

0.4 Fabrication - standard EBL method similar to NTT group

S/D and contacts

1. SOI 20 - 100 nm.
2. photolith for alignment marks.

3. Etch alignment mark holes, S/D holes in SiO_2 with TMAH, HF.
4. S/D implanted.
5. RCA clean to remove metal ions, etch off oxide.
6. Anneal dry N_2 950 C 30 min

Si nanowire

7. EBL for wires (negative polarity?)
8. Etch Si down to box with RIE.
9. remove resist.

gates

10. gate oxide 40 nm at 1000 C.
11. deposit degenerately-doped poly-Si.
12. EBL for lower gates (negative polarity?).
13. RIE poly-Si down to gate oxide.
14. CVD or thermal oxide for lower/upper gate isolation.
15. deposit degenerately-doped poly-Si.
16. EBL for upper gates (negative polarity?).

17. RIE poly-Si down to gate oxide.

passivation/contacts

18. metallization for wires and gates to contact pads. Our standard geometry: 24 pads around a 0.8 cm square.
19. wirebond (at NIST).

0.5 Fabrication - TMAH etching method similar to U. Tokyo group

S/D and contacts

1. SOI 20 - 100 nm.
2. photolith for alignment marks.
3. Etch alignment mark holes, S/D holes in SiO_2 with TMAH, HF.
4. S/D implanted.
5. RCA clean to remove metal ions, etch off oxide.
6. Anneal dry N_2 950 C 30 min

Si nanowire

7. Deposit Si_3N_4 (10 nm) by LPCVD
8. photolith to open holes for first TMAH etch – align to SiO_2 marks.
9. Etch away edges of Si_3N_4 along (110) with CF_4 50 nm/min, or H_3PO_4 at 180 C.
10. liftoff PR in acetone
11. TMAH at 75 C for first edge
12. Selectively oxidize edges – 30 nm at 1000 C
13. Blanket etch Si_3N_4 with CF_4
14. TMAH again forms Si wires - **need to control pH?**

gates

15. gate oxide 40 nm at 1000 C.
16. deposit degenerately-doped poly-Si.
17. EBL for lower gates (negative polarity?).
18. RIE poly-Si down to gate oxide.
19. CVD or thermal oxide for lower/upper gate isolation.
20. deposit degenerately-doped poly-Si.
21. EBL for upper gates (negative polarity?).
22. RIE poly-Si down to gate oxide.

passivation/contacts

23. metallization for wires and gates to contact pads. Our standard geometry: 24 pads around a 0.8 cm square.
24. wirebond (at NIST).

References

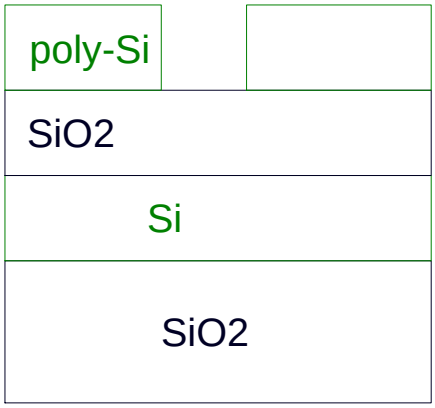
[1] C. Single, F. E. Prins, and D. P. Kern. "Simultaneous operation of two adjacent double dots in silicon". *Appl. Phys. Lett.*, 78:1421 – 3, 2001.

[2] B. T. Lee et al. "Fabrication of a dual-gate-controlled Coulomb blockade transistor based on a silicon-on-insulator structure". *Semicond. Sci. Technol.*, 13:1463 – 7, 1998.

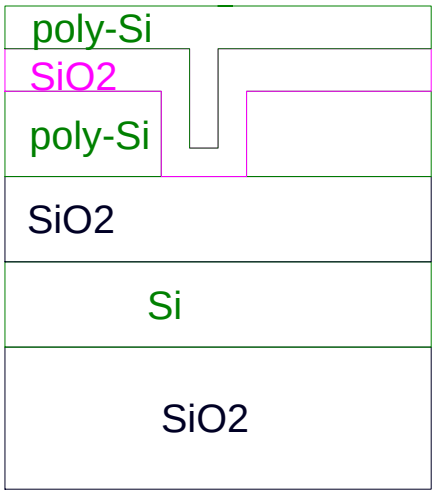
[3] J. W. Park et al. "Enhancement of Coulomb blockade and tunability by multidot coupling in a silicon-on-insulator-based single-electron transistor". *Appl. Phys. Lett.*, 75:566 – 8, 1999.

implant

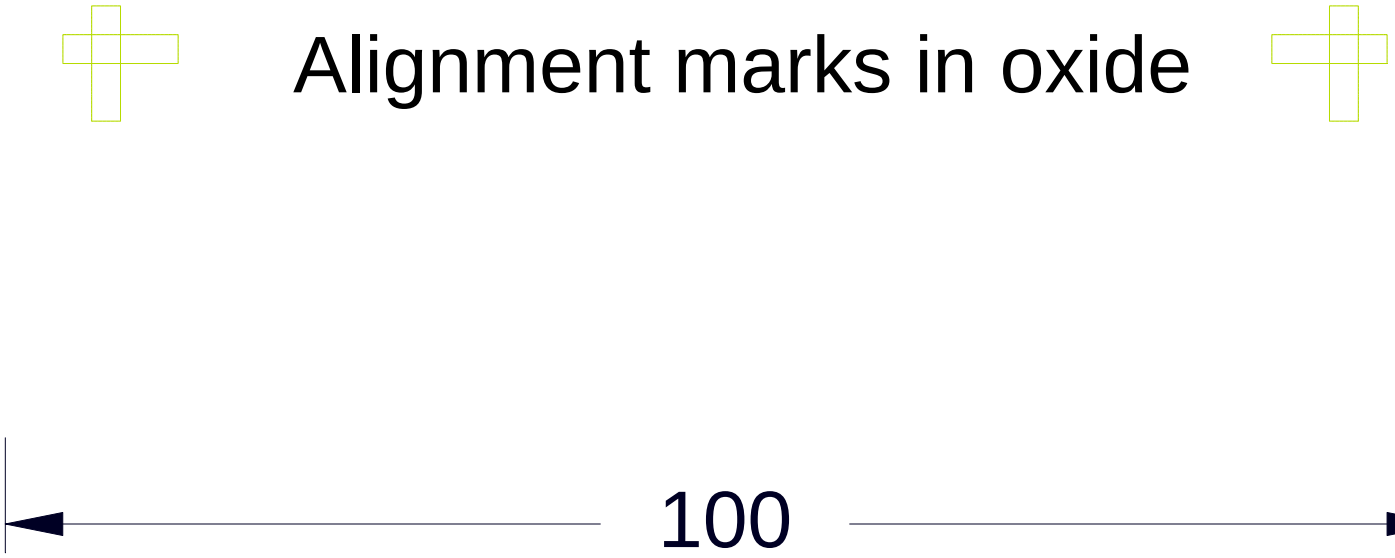
etch wire



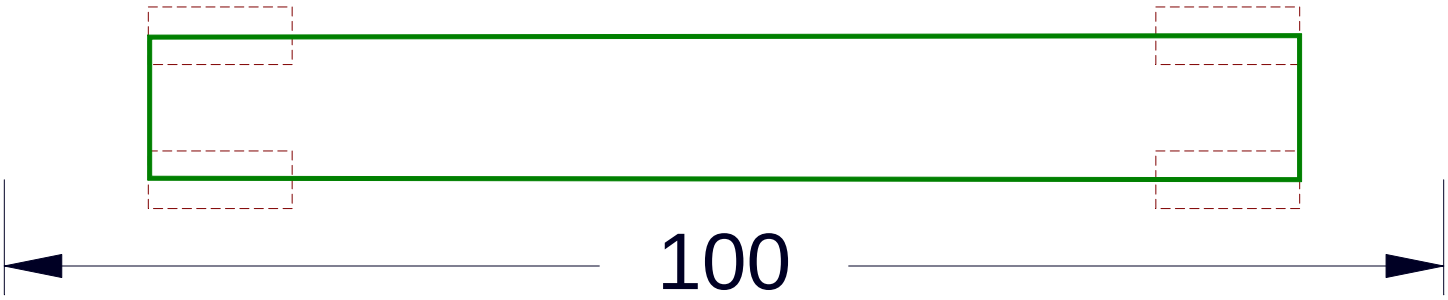
lower gate



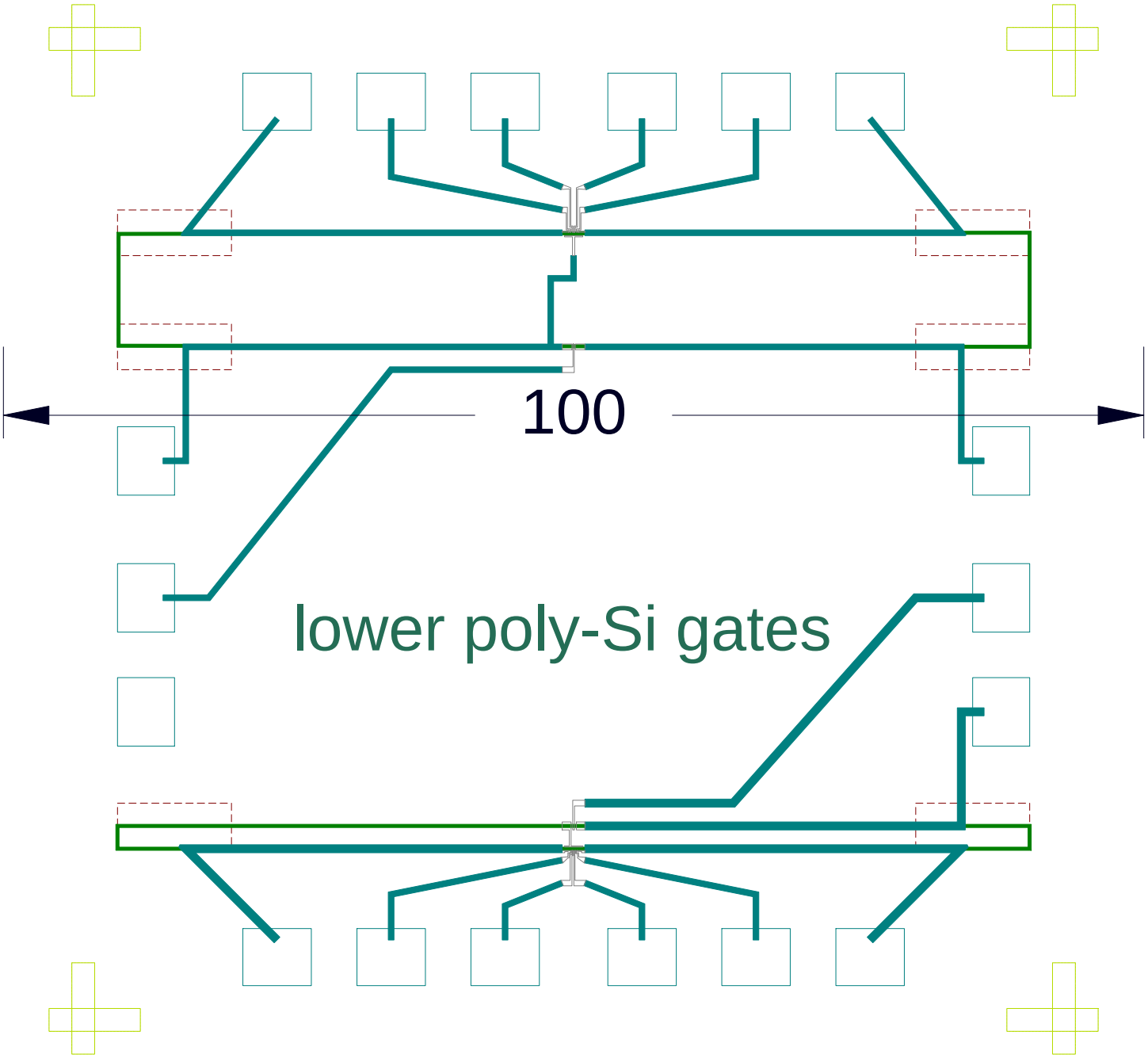
upper gate

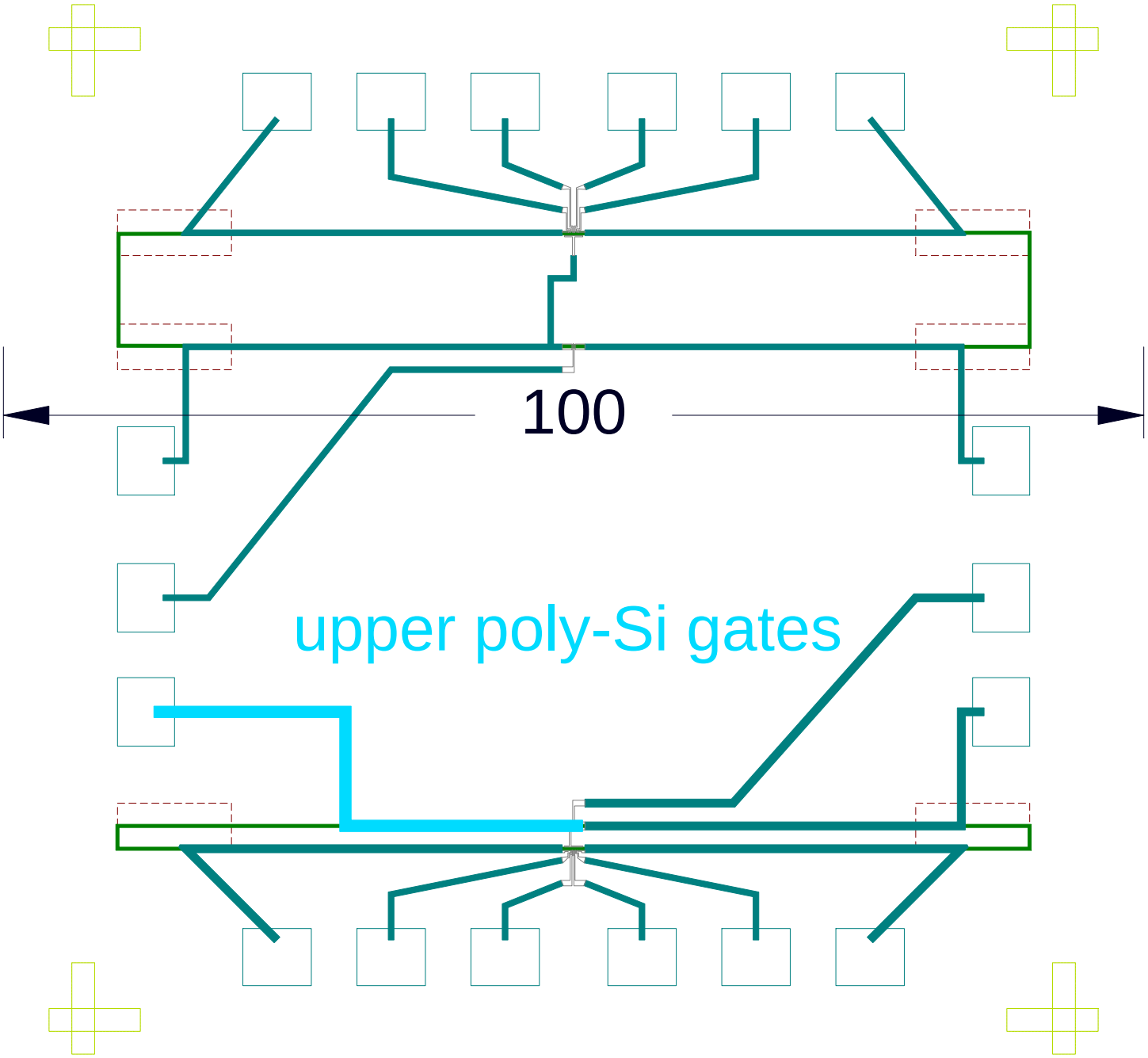

Alignment marks in oxide
100

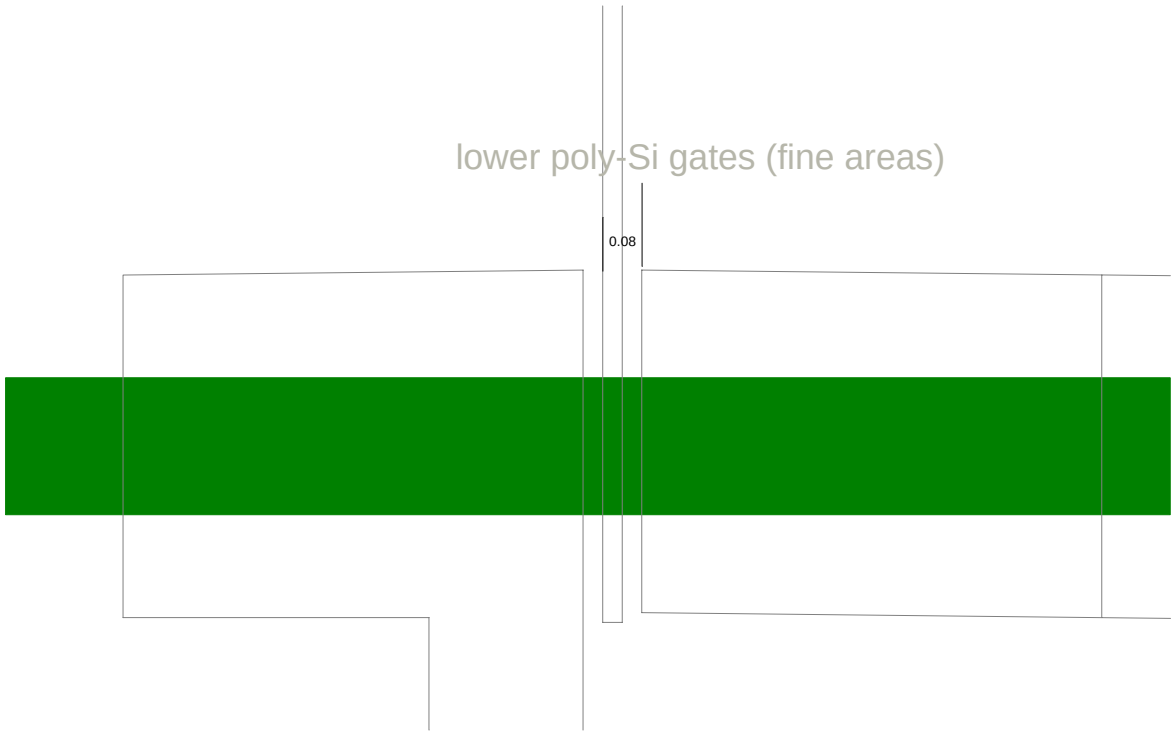
implant S/D through oxide



Si nanowire from TMAH etching or EBL


100
lower poly-Si gates


100
upper poly-Si gates


lower poly-Si gates (fine areas)
0.08